WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a protective circuit including

a plurality of protective elements connected in parallel between a signal line and a power supply line, each including

a plurality of metal oxide semiconductor (MOS) transistors, and

a plurality of resistors, wherein, in the respective protective elements, drains of the MOS transistors are connected to the signal line that establishes a connection between a pad and an internal circuit through the resistors, and sources of the MOS transistors are connected to the power supply line,

wherein a resistance of the resistors in each of the protective elements is gradually decreased from the pad toward the internal circuit.

2. The semiconductor integrated circuit device according to claim 1, wherein the resistance of the resistors becomes lower from the pad toward the internal circuit according to a parasitic resistance of the signal line.

3. The semiconductor integrated circuit device according to claim 1, wherein the resistors are polysilicon resistors formed on a semiconductor substrate.

4. The semiconductor integrated circuit device according to claim 1, wherein the resistors are well resistors formed on a semiconductor substrate.

5. The semiconductor integrated circuit device according to claim 1, wherein the resistors are silicide resistors formed on a semiconductor substrate.

6. The semiconductor integrated circuit device according to claim 1, wherein the resistors are silicide blocks formed on a semiconductor substrate.

7. The semiconductor integrated circuit device according to claim 1, wherein the resistors are formed with elements whose resistance is changed by changing at least one of a length and a width of drain wiring connected to the signal line.

8. The semiconductor integrated circuit device according to claim 1, wherein the resistors are formed with elements whose resistance is changed by changing a number of contacts that establish electric connections between drain wirings connected to the signal line and a drain area.

9. The semiconductor integrated circuit device according to claim 1, wherein the resistors are elements each formed with a combination of

at least two selected from a group consisting of a) polysilicon resistors, b) well resistors, c) silicide resistors, and d) silicide blocks.

10. The semiconductor integrated circuit device according to claim 1, wherein when decreasing the resistance of the resistors in each of the protective elements, the resistance is gradually decreased with at least every other unit among the resistors from the pad toward the internal circuit.

11. A semiconductor integrated circuit device comprising:

a narrow pitch input-output (I/O) circuit having a system of obtaining an I/O circuit with a desired configuration by changing wirings connecting a plurality of transistors disposed in the I/O circuit, the narrow pitch I/O circuit including

a protective circuit including

a plurality of protective elements connected in parallel between a signal line and a power supply line, each including

a plurality of metal oxide semiconductor (MOS) transistors, and

a plurality of resistors, wherein, in the respective protective elements, drains of the MOS transistors are connected to the signal line that establishes a connection between a pad and an internal circuit through the resistors, and sources of the MOS transistors are connected to the power supply line, wherein a resistance of the resistors in each of the protective elements is gradually decreased from

the pad toward the internal circuit.

12. A semiconductor integrated circuit device comprising:

a protective circuit including

a plurality of protective elements connected in parallel between a signal line and a power supply line, each including

a plurality of metal oxide semiconductor (MOS) transistors, and

a plurality of resistors, wherein, in the respective protective elements, drains of the MOS transistors are connected to the signal line that establishes a connection between a pad and an internal circuit through the resistors, and sources of the MOS transistors are connected to the power supply line,

wherein a resistance of the resistors in each of the protective elements is lower than a resistance of resistors in a first adjacent protective element on a side of the pad, and is higher than a resistance of resistors in a second adjacent protective element on a side of the internal circuit.

13. The semiconductor integrated circuit device according to claim 12, wherein the resistance of the resistors becomes lower from the pad toward the internal circuit according to a parasitic resistance of the signal line.

14. The semiconductor integrated circuit device according to claim

12, wherein the resistors are polysilicon resistors formed on a semiconductor substrate.

15. The semiconductor integrated circuit device according to claim 12, wherein the resistors are well resistors formed on a semiconductor substrate.

16. The semiconductor integrated circuit device according to claim 12, wherein the resistors are silicide resistors formed on a semiconductor substrate.

17. The semiconductor integrated circuit device according to claim 12, wherein the resistors are silicide blocks formed on a semiconductor substrate.

18. The semiconductor integrated circuit device according to claim 12, wherein the resistors are formed with elements whose resistance is changed by changing at least one of a length and a width of drain wiring connected to the signal line.

19. The semiconductor integrated circuit device according to claim 12, wherein the resistors are formed with elements whose resistance is changed by changing a number of contacts that establish electric connections between drain wirings connected to the signal line and a drain area.

20. The semiconductor integrated circuit device according to claim 12, wherein the resistors are elements each formed with a combination of at least two among those: a) polysilicon resistors, b) well resistors, c) silicide resistors, and d) silicide blocks.

21. A semiconductor integrated circuit device comprising:

a narrow pitch input-output (I/O) circuit having a system of obtaining an I/O circuit with a desired configuration by changing wirings connecting a plurality of transistors disposed in the I/O circuit, the narrow pitch I/O circuit including

a protective circuit including

a plurality of protective elements connected in parallel between a signal line and a power supply line, each including

a plurality of metal oxide semiconductor (MOS) transistors, and

a plurality of resistors, wherein, in the respective protective elements, drains of the MOS transistors are connected to the signal line that establishes a connection between a pad and an internal circuit through the resistors, and sources of the MOS transistors are connected to the power supply line, wherein a resistance of the resistors in each of the protective elements is lower than a resistance of resistors in a first adjacent protective element on a side of the pad, and is higher than a resistance of resistors in a second adjacent protective element on a side of the internal circuit.